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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/816,018	03/31/2004	Marijan Persun	42P14976X	2617
8791	7590	09/29/2005	EXAMINER	
BLAKELY SOKOLOFF TAYLOR & ZAFMAN 12400 WILSHIRE BOULEVARD SEVENTH FLOOR LOS ANGELES, CA 90025-1030			NGUYEN, TUNG X	
			ART UNIT	PAPER NUMBER
			2829	

DATE MAILED: 09/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-7 are rejected under 35 U.S.C. 102(b) as being anticipated by Itoh et al. (u.s.p 5,410,278).

As to claim 1, Itoh et al. disclose in Figs. 1-3, an apparatus comprising:

An n-type (14b of figure 3a) and p-type device (14a of figure 3a) coupled between first (at P) and second supply voltages (at N) at a terminal; and an output node coupled to the terminal (input of another inverter (11a, b, c)), during operation of the apparatus, to provide an output signal having a switching delay (11a, b, c of figure 3a) in only one direction that is directly proportional to the leakage current (12 of figure 1) of one of the n-type and p-type devices.

As to claim 2, Itoh et al. disclose in Figs. 1-3, the n-type (14b of figure 3a) and p-type (14a of figure 3a) devices are coupled to function as an inverter (11 a, b, c of figure 3a).

As to claims 3-4, Itoh et al. disclose in Figs 1-3, the drains of the n-type (14b of figure 3a) and p-type devices (14a of figure 3a) are coupled to each other at the terminal; a gate of a first one of the n-type and p-type devices (14a, 14b of figure 3a) is

Art Unit: 2829

coupled to receive an input signal (11a, 11b, 11c of figure 3a); and a gate of a second one of the n-type and p-type devices (11b of figure 3a) is coupled to receive a bias voltage (output of the 11a of figure 3a) during operation that results in the gate-to-source voltage of the second device (11b of figure 3a) being less than the threshold voltage of the second device.

As to claims 5-6, Itoh et al. disclose in Figs. 1-3, a gate of a first one of the n-type (14b of figure 3a) and p-type devices (14a of figure 3a) is coupled to receive an input signal (feedback from 11c of figure 1, and figure 3a); and a gate of a second one of the n-type (14b of figure 3a) and p-type device (14a of figure 3a) is coupled to the output node (via 11a) and the source and drain of the second one of the n-type (11b).

As to claim 7, Itoh et al. disclose in Figs. 1-3, an apparatus comprising: a ring oscillator (11 of figure 1) including at least one leakage inverter (11 a, b, c of figure 1) to provide an inverted output signal (after each inverter 11 of figure 1) having a signal transition delay in one direction that is proportional to a leakage current (12 of figure 1) of a device of a first leakage inverter, and one or more static stages (11a, 11b, or 11c of figure 1), the ring oscillator to provide an oscillator output signal (output 11c of figure 1).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 8-11, 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Itoh et al. (u.s.p 5,410,278), in view of Deal et al. (u.s.p 6,657,504).

As to claim 8, Itoh et al. disclose in Fig. 3a, the at least one leakage inverter (11a, 11b, 11c of figure 13a) includes a leaky device (14a, or 14b of figure 3a) having a gate for receiving a feed back voltage (output from 11c and feed back to 11a of figure 1) during operation that provides a sub-threshold gate-to-source voltage, and wherein the leakage current is a drain leakage current (col. 1, lines 59-65). Itoh et al., is silent about the gate for receiving a bias voltage. However, Deal et al. disclose in Fig. 1, the gate (12 of figure 1) for receiving a bias voltage (ENABLE of 12) to enable the inverters in the ring oscillator. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the system of Itoh et al., and provide the gate for receiving a bias voltage (ENABLE of 12) to enable the inverters in the ring oscillator.

As to claim 9, Itoh et al. disclose in Fig. 1, the gate of the leaky device (12-15 of figure 1) is coupled to receive an enable signal (ENABLE of 12), the leaky device to be turned on in response to the enable signal being deasserted.

As to claims 10-11, Itoh et al. disclose in Fig. 3a, the at least one leakage inverter (14a, or 14b of figure 3a) includes a leaky device (14a, b, c) having a source (P of figure 3a) and drain (P of figure 3a) coupled to receive a supply voltage (at the source of P) and a gate (11a of figure 1, and 3a) coupled to an output node of the leakage inverter (11b or c of figure 1, 3a), and wherein the leakage current is a gate leakage current (col. 1, lines 59-65).

As to claim 12, Deal et al. disclose in Fig. 1, the ring oscillator includes at least three leakage inverters, and wherein a frequency of the oscillating output signal varies in proportion to the leakage current of the device (col. 3, lines 50-55).

5. Claims 26-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Deal et al. (u.s.p 6,657,504), in view of Itoh et al. (u.s.p 5,410,278).

As to claim 26, Deal et al. disclose in Fig. 1, an method comprising: detecting a frequency of a leakage ring oscillator on an integrated circuit (see abstract, and col. 3, lines 32-37); the leakage ring oscillator including at least a first leakage inverter (13-15 of figure 1) to provide an inverted output (output of 13-15 of figure 1) signal having a transition delay in one direction that is proportional to a leakage current of a device of the leakage inverter over a first temperature range; and determining one of a local temperature or relative leakage current in response to the detected frequency (col. 3, lines 50-55). Deal et al., do not disclose the step of at least a first leakage inverter to provide an inverted output signal having a transition delay in one direction that is proportional to a leakage current of a device of the leakage inverter. However, Itoh et al. disclose in Figs. 1-3a, at least a first leakage inverter to provide an inverted output signal having a transition delay in one direction that is proportional to a leakage current of a device of the leakage inverter (via 12 of figure 1). Therefore, It would have been obvious to a person having ordinary skill in the art at the time the invention was made to system of Deal et al., and provide the leakage current generating part, as taught by Itoh et al. for detecting the leakage current generating from the leakage inverters in the ring oscillator (col. 3, lines 5-10).

Art Unit: 2829

As to claim 27, Deal et al. disclose in Fig. 1, wherein determining comprising: accessing data indicating leakage ring oscillator frequency versus at least one of temperature and leakage current (col. 3, lines 50-55).

As to claim 28, Deal et al. disclose in Fig. 1, characterizing each of the leakage ring oscillator at different temperatures; and developing a look-up table indicating frequency of the oscillating output signal versus temperature (col. 3, lines 50-55).

Allowable Subject Matter

6. Claims 13-19, and 20-25 are allowed.

7. The following is an examiner's statement of reasons for allowance:

As to claims 13-19, the prior art does not disclose or suggest the leakage ring oscillator including at least a first leakage inverter including a leaky device, the leaky device to be substantially fully turned on in response to the enable signal being deasserted; in combination with the other claimed features.

As to claims 20-25, the prior art does not disclose or suggest an integrated circuit comprising a plurality of leakage ring oscillators wherein each of the plurality of leakage ring oscillators to provide an oscillating output, a frequency of the respective oscillators output signal to indicate at least one of a local temperature and leakage current; in combination with the other claimed features.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably

Art Unit: 2829

accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

8. Applicant's arguments filed 7/05/05 have been fully considered but they are not persuasive.

In re-pages 9-11, Applicant argues that Itoh does not teach or suggest a leakage inverter provides an inverted output signal that has a transition in one direction that is proportional to the leakage current of a device in the leakage inverter itself.

In response, Examiner respectfully disagrees with Applicant about the issue for the following reasons: It appears that the leakage current generated from memory cell would inherently include a leakage current of the inverter itself.

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.


Art Unit: 2829

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tung X. Nguyen whose telephone number is (571) 272-1967. The examiner can normally be reached on 8:30am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nestor Ramirez can be reached on (571) 272-2034. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TN
9/26/05


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